# PACE INSTITUTE OF TECHNOLOGY \& SCIENCES::ONGOLE (AUTONOMOUS) 

II B.TECH I SEMESTER END SUPPLEMENTARY EXAMINATIONS, MARCH/APRIL - 2023
DIGITAL LOGIC DESIGN
(Common to CSE, CSE(IOTCSBT) Branches)
Time: 3 hours
Max. Marks: 60
Note: Question Paper consists of Two parts (Part-A and Part-B)
PART-A
Answer all the questions in Part-A $(5 \mathrm{X} 2=10 \mathrm{M})$

| Q.No. |  | Questions | Marks | CO | KL |
| :---: | :---: | :--- | :---: | :---: | :---: |
| 1 | a) | Convert gray code 10101110 into its binary equivalent. | $[2 \mathrm{M}]$ | 1 |  |
|  | b) | Draw the NOR gate using NAND gate. | $[2 \mathrm{M}]$ | 2 |  |
|  | c) | Draw the K map for 4 variables. | $[2 \mathrm{M}]$ | 3 |  |
|  | d) | What is the difference between decoder and encoder? | $[2 \mathrm{M}]$ | 4 |  |
|  | e) | Draw the circuit diagram for SR flip flop. | $[2 \mathrm{M}]$ | 5 |  |

PART-B
Answer One Question from each UNIT (5X10=50M)

| Q.No. |  | Questions | Marks | CO | KL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT-I |  |  |  |  |  |
| 2. | a) | Convert the following to Decimal and then to Octal. <br> i) $125 \mathrm{~F}_{16}$ <br> ii) $10010011_{2}$ | [5M] | 1 |  |
|  | b) | The binary numbers listed have a sign bit in the left most position and if negative, are in 1's complement form. Perform the arithmetic operations <br> i) $101011+111000$ <br> ii) $001110+110010$ | [5M] | 1 |  |
| OR |  |  |  |  |  |
| 3. | a) |  | [5M] | 1 |  |
|  | b) | A receiver with even parity hamming code receives the data 1110110. Determine the correct code. | [5M] | 1 |  |
| UNIT-II |  |  |  |  |  |
| 4. | a) | State duality theorem. List Boolean laws and their duals. | [5M] | 2 |  |
|  | b) | Test the given expression into canonical SOP form <br> i) $f=A B+B C+C A$ <br> ii) $f=A+A B+A B C$ | [5M] | 2 |  |
| OR |  |  |  |  |  |
| 5. | a) | Reduce the Boolean expression <br> i) $F=(\overline{\bar{X}} \cdot \bar{Y}+Z)+Z+X Y+W Z$ into three literals. <br> ii) $F=\bar{A} \cdot \bar{C}+A B C+A \cdot \bar{C}+A \cdot \bar{B}$ into two literals. | [5M] | 2 |  |
|  | b) | Implement the following function F with the following two levels forms <br> a) NAND-AND <br> b) AND-NOR $\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\sum(0,1,2,3,4,8,9,12) .$ | [5M] | 2 |  |
| UNIT-III |  |  |  |  |  |
| 6. | a) | Obtain minimal SOP expression for the given Boolean function using Kmap, and realize using NAND gates. $\mathrm{F}=\sum \mathrm{m}(0,1,4,5,6,7,9,11,15)+\sum \mathrm{d}(10,14)$ | [5M] | 3 |  |


|  | b) | Simplify the following Boolean expressions using K-map and implement using NOR gates. $\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\mathrm{AB} \mathrm{C}^{\prime}+\mathrm{AC}+\mathrm{A}^{\prime} \mathrm{CD}^{\prime}$ | [5M] | 3 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OR |  |  |  |  |  |
| 7. | a) | Reduce the following using k-map and implement it in NAND logic $\mathrm{F}=\pi \mathrm{M}(0,1,2,3,4,7)$ | [5M] | 3 |  |
|  | b) | Obtain minimal SOP expression for the Boolean function $\mathrm{F}=\sum \mathrm{m}(0,5,7,8,9,10,11,14,15)$ using K -map, and realize using NAND gates. | [5M] | 3 |  |
| UNIT-IV |  |  |  |  |  |
| 8. | a) | Design a combinational logic circuit for full-adder and give its applications | [5M] | 4 |  |
|  | b) | Realize 5-to-32 line decoder using one 2-to-4 and four 3-to-8 decoders | [5M] | 4 |  |
| OR |  |  |  |  |  |
| 9. | a) | Write about combinational logic circuit for BCD adder. | [5M] | 4 |  |
|  | b) | Draw 16x1 multiplexer tree using 4x1 multiplexer. | [5M] | 4 |  |
| UNIT-V |  |  |  |  |  |
| 10. | a) | Discuss the T- flip flop \& D - flip flop using truth table and circuit. | [5M] | 5 |  |
|  | b) | Write about Master Slave JK flip flop | [5M] | 5 |  |
| OR |  |  |  |  |  |
| 11. | a) | Draw the circuit of JK flip-flop and explain its operation with the help of its function table. | [5M] | 5 |  |
|  | b) | Design a Mod-8 asynchronous up counter. | [5M] | 5 |  |

